

Cover Time On Regular Graph

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March 8, 2013

1 Abstract

Doyle & Snell (1984) [2] exposed many interesting connections between random walks and electrical network theory, by viewing an undirected graph as an electrical network in which each edge of the graph is replaced by an unit resistance. Their work and other follower's work provide many useful tools from electrical network theory that can offer intuitive understanding of random walk behavior on the graph. Some counter-intuitive phenomenon in random walk can be explained with these new tools. One of the counter-intuitive examples is that, under certain circumstances, the cover time will increase by adding edges to the graph. For example, we can transform a line graph to a lollipop graph by adding edges to the original graph, yet with the cover time increased. Before using this electrical network language, we are not able to describe what has changed in the graph after adding edges in a way both quantitatively and qualitatively. We will show effective resistance, a tool borrowed from the electrical network theory, will give a good explanation of the phenomenon. And we will use this tool to study random walks on regular graph, a sharper($O(n^2)$) upper bound for cover time on d-regular graph was found with this tool.

2 Introduction

In computer science, graph traversal is the problem of visiting all the nodes in a graph. It is well known that deterministic solutions such as DFS or BFS can be achieved with a time complexity of $O(|E|)$ and space complexity $O(|V|)$ (for a connected graph $G=(V,E)$). Deterministically

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following a $O(n^3)$ universal sequence, we can also traverse the graph. For the same problem, random walk just needs $O(1)$ space(it just needs to keep track of the current vertex visited), yet the Cover Time is bounded by $O(|V||E|)$ [1]. In this paper, the main subject was to show how to utilize several electrical theory tools to better capture the structural constraints of the network and thus find better bounds for the cover time. In section 3, we will present several tools in the arsenal to solve this problem. In section 4, 5, 6, We will use those tools to study 3 important electrical properties, $R_{st}, R_{span}, \delta_{st}$ (excess resistance) in d-regular graph. In section 7, we will use all these electrical languages to find stronger bounds of cover time.

3 Random walk and electrical network equivalencies

In electrical theory, the **electrical resistance** of an **electrical conductor** is the *opposition* to the passage of an electric current through that conductor; the inverse quantity is **electrical conductance**, the *ease* at which an electric current passes. Electrical resistance shares some conceptual parallels with the mechanical notion of friction. [6].

Since Doyle & Snell (1984) [2], many equivalences between electric networks and random walks on graph has widely been known. Since the **electrical resistance** captures the *opposition* of electrical current passage, in its random walk equivalency, we want to study how this electrical property **electrical resistance** relates to the difficulty of finishing a random walk task, i.e. the length a random walk take to finish the task. For example, the difficulty of hitting some node, visiting all nodes, etc. Among all of these, a most impressive result relating the random walk lengths to electrical network resistance is captured by the commute time. The resistance in the electrical network actually can give exact values for commute times on corresponding graph. In this section, we study resistance values of d-regular graph and show how they can help use get better estimates of cover time.

Let $\mathbf{G}=(\mathbf{V},\mathbf{E})$ be an d-regular undirected connected graph with $|V| = n$ vertices and $|E| = m$ edges. Let $\mathbf{N}(\mathbf{G})$ denote the corresponding electrical network with each edge replaced by a unit resistor.

Definition 3.1. $\forall s, t \in V$, the **hitting time** $\mathbf{H}(\mathbf{s},\mathbf{t})$ is defined as the expected number of steps to first visit t from s . The **commute time** $\mathbf{C}(\mathbf{s},\mathbf{t}) = H(s,t) + H(t,s)$ which denotes the expected time the random walk take to traverse from s to t and then back to s .

Definition 3.2. $\forall u \in V$, the **cover time** from u is defined as $\text{Cov}(\mathbf{G}, \mathbf{u})$, expected number of steps to visit all vertices starting from u . $\text{Cov}(\mathbf{G})$, the cover time of the graph, is defined as $\max_u \text{Cov}(\mathbf{G}, u)$ over all vertices u .

Definition 3.3. $\forall s, t \in V$, R_{st} denotes the **effective resistance** between the corresponding nodes in $\mathbf{N}(\mathbf{G})$, i.e., the potential difference required between \mathbf{s} and \mathbf{t} to send a current of one amp from \mathbf{s} to \mathbf{t} .

Definition 3.4. effective resistance of spanning tree R_{span} denotes the sum of effective resistances of all edges in the tree,

Definition 3.5. effective resistance of the graph \mathbf{G} R_G denotes maximum effective resistance between any pair of vertices.

After introducing these concepts and properties, we begin our study and solving our doubts: in a intuitive way, if more *opposition* (effective resistance) exists between vertices \mathbf{s} and \mathbf{t} , is it more difficult task for an random walker to reach each other? With the results from [3], we will answer this question with an affirmative answer.

Lemma 3.1. For all s, t , the **commute time** $\mathbf{C}(\mathbf{u}, \mathbf{v}) = 2mR_{st}$.

In addition, with results from [3], we are able to use commute time to upper bound the cover time.

Theorem 3.2. For any connected graph G , **cover time** $\text{Cov}(\mathbf{G}) \leq 2mR_{\text{span}}$

Serial Connection : Resistors that are connected in series can be replaced by a single resistor whose resistance is the sum of the resistances.

Parallel Connection : Resistors that are connected in parallel can be replaced by a single resistor whose conductance is the sum of the conductances.

Rayleigh's Short-Cut Principle: Resistance is never raised by lowering the resistance on an edge, e.g., by “shorting” two nodes together, and is never lowered by raising the resistance on an edge, e.g., by “cutting” it. Similarly, resistance is never lowered by “cutting” a node, leaving each incident edge attached to only one of the two “halves” of the node.

Foster's theorem: For connected graph $G=(V,E)$, the sum of the effective resistances along the edges of G satisfies: $\sum_{(s,t) \in E} R_{st} = n - 1$

The upper bound for the cover time in this section was developed by [1]. It's obvious that the proof gives a rather loose upper bound which utilized little information on the structure of the graph except the undirected nature of the graph and the number of edges. With all these tools introduced in this section we begin to study to better our understanding of random walk behaviors on d-regular graph and its electrical network equivalences [4].

4 R_{st} on d-regular graph

Proposition 4.1. *The effective resistance between any two vertices $u, v \in V$ satisfies:*

$$R_{uv} \geq \frac{2}{d+1}$$

Proof. To use **Rayleigh's Short-Cut Principle**, separate this problem into 2 cases:

case 1: if $(u, v) \notin E$:

Construct from G a new graph $G' = (E', V')$ by Collapsing all vertices of G which are not connected with u or v to a single vertex w, we will have: $V' = \{u, v, w\}$. $|E'| = d + d$.

By parallel connection,

$$R'_{uw} = \frac{1}{d}. \quad R'_{wv} = \frac{1}{d}.$$

By serial connection,

$$R'_{uv} = R'_{uw} + R'_{wv} = \frac{2}{d}$$

By the shortcut principle,

$$R_{uv} \geq R'_{uv}$$

Based on the analysis:

$$R_{uv} \geq \frac{2}{d}.$$

case 2: if $(u, v) \in E$:

Under this circumstances, if we can replace the edge (u,v) to another electrical equivalency and with the two vertices dis-connected, we can run similar analysis as case 1 did on case 2. we modify the edge(u,v) as Fig1 shows (then the degree of each of the vertices u and v increased by 1): Construct another graph G' in the similar previous way by collapsing all vertices which is not connected with u or v to a single vertex w. Based on the previous analysis:

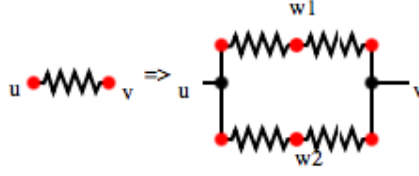


Figure 1: serial to parallel.

$$R_{uv} \geq \frac{2}{d+1}.$$

□

5 Excess resistance

Definition 5.1. *The excess resistance δ_{uv} of edge $(u, v) \in E$ is defined by:*

$$\delta_{uv} = R_{uv} - \left(\frac{2}{d+1}\right)$$

Observe that by **Proposition 4.1**, $\delta_{uv} \geq 0$.

The following identity plays a fundamental role in turning structural constraints to better **effective electrical resistance** upper bounds:

Lemma 5.1. *: On d -regular connected graph $G=(V,E)$, the sum of **excess resistances** along its edges is a constant and satisfies: $\sum_{(u,v) \in E} \delta[(u, v)] = n - 1 - \frac{nd}{d+1}$*

Proof. From the definition, we have $\sum_{(u,v) \in E} \delta[(u, v)] = \sum_{(u,v) \in E} (R(u, v) - \frac{2}{d+1})$

G is a regular graph, we have $m = |E| = \frac{nd}{2}$

From Foster's theorem, we have $\sum_{(u,v) \in E} R(u, v) = n-1$

Re-arrange the formulas above, we can get the proof.

6 R_{span} on d -regular graph

We now turn to bound R_{span} , the resistance of the spanning tree of minimum resistance.

Theorem 6.1. *: In connected d -regular graphs, the resistance of any spanning tree T satisfies:*

$$\frac{2(n-1)}{(d+1)} \leq R(T) \leq \frac{3(n-1)}{(d+1)}$$

Proof. From the fact that any spanning tree in graph G has $n-1$ edges, and the lower bounds on the effective resistance of an edge, we have the lower bound:

$$R(T) \geq \frac{2}{(d+1)} \times (n-1)$$

According to the definition of **excessing resistance**, we have

$$R_{span} = (n-1) \times \frac{2}{d+1} + \sum_{(u,v) \in T} \delta[(u,v)]$$

From the fact that any spanning tree has less edges than the graph itself.

$$\sum_{(u,v) \in T} \delta[(u,v)] \leq \sum_{(u,v) \in E} \delta[(u,v)],$$

According to Lemma 4 $\sum_{(u,v) \in E} \delta[(u,v)]$ is a constant, we get the upper bound :

$$R_{span} \leq \frac{3(n-1)}{(d+1)}$$

Observe the relationship, you can easily get an idea that all spanning trees in a regular graph have roughly the same effective resistance.

□

7 Cover time

In [3], the upper bound for cover time was reached through the use of commute time measure and the identity $Cov(G) \leq 2mR_{span}$. The commute time measure naturally leads us to study R_{span} on the corresponding electrical network. We also show how to utilize R_{st} to study R_{span} . In addition, we show how to use a designed excess resistance measure to capture the interaction between lower bound for R_{st} and constraints of the network from Foster's theorem, which finally leads to a better upper bound for R_{span} and $O(n^2)$ cover time upper bound.

In [5] a sharper bound $2n^2$ of cover time for d -regular graph was found. One distinction between the two methods deserving a final mention is that the later method mainly depends on a well applying of another random walk tool: **difference time**.

$$\text{commute time } C(s,t) = H(s,t) + H(t,s).$$

$$\text{difference time } D(s,t) = H(s,t) - H(t,s).$$

8 Summary

There are a lot of techniques to study the cover time problem. We mainly study in this paper the importance of good tools in getting better observation of a mathematical problem. The deep connections between random walk on graph and electrical network enabled the transfer of tools in these two fields and shed lights to each other.

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